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10/806,866	03/22/2004	Robert Tod Dimpsey	AUS920040065US1	2686

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,866	DIMPSEY ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/5/06, 11/10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed January 5, 2007 in response to the Office action dated October 10, 2006. Claims 1-5, 12-16, and 18-22 have been amended. Claims 9-11 have been cancelled. Claims 1-8 and 12-23 are pending in this application.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

1. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statements dated October 5, 2006 and November 11, 2006 are acknowledged by the Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by the Examiner is attached to the instant Office action.

OBJECTIONS

Specification

2. In the section entitled "Cross Reference to Related Applications" Applicant must properly identify all co-pending applications with their corresponding application numbers (i.e. serial numbers).

REJECTIONS NOT BASED ON PRIOR ART

Double Patenting

3. In view of Applicant's terminal disclaimer filed with the amendment, the provisional double-patenting rejections to **claims 1-3, 6-7, 9, 12-14, 17-20, and 23** have been withdrawn.

Claim Rejections - 35 USC § 101

4. In view of Applicant's amendment, the 101 rejections to **claims 18-23** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 4-8, 12, 15-18, and 21-23 are rejected under U.S.C. 102(e) as being anticipated by Damron (U.S. Patent 6,782,454).

7. **As per claims 1 and 18**, Damron discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction (col. 4, lines 58-61; col. 5, lines 17-24; Fig. 1, element 175; Fig. 3, element 220); *It should be noted that computer program product in claims 18-23 executes the exact same functions as the methods in claims 1-6. Therefore, any references that teach claims 1-6 also teach the corresponding claims 18-23. It should also be noted that the "prefetch request" is analogous to the "instruction", the "prefetch engine" is analogous to the "processing unit", and the "starting address of a node, an offset value, and a termination value" all are analogous to the "metadata."*

responsive to determination of metadata being present for the instruction, determining whether data is to be prefetched (col. 5, lines 27-35; Fig. 3, element 230); *It should be noted that "determining whether a termination condition has been satisfied" is analogous to "determining whether data is to be prefetched." Data is prefetched until the termination condition is met.*

and responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor (col. 5, lines 24-26 and 35-42; Fig. 3, elements 225 and 235). *It should be noted that responsive to the termination condition not being met, data is prefetched.*

8. **As per claims 4 and 21**, Damron discloses retrieving the data from within the data structure using a pointer and an offset value (col. 5, lines 20-21). *It should be noted that the "starting address of a node" is analogous to a "pointer."*

9. **As per claims 5 and 22**, Damron retrieving the data from the data structure using an address (col. 5, lines 20-21).

10. **As per claims 6 and 23**, Damron discloses the processor unit is selected from one of an instruction cache or a load/store unit (col. 4, lines 58-61; Fig. 1, element 175). *It should be noted that the "prefetch engine" is analogous to a "load/store unit."*

11. **As per claim 7**, Damron discloses the cache is an instruction cache (col. 4, lines 53-54).

12. **As per claim 8**, Damron discloses the metadata includes the pointer and the offset value (col. 5, lines 20-21). *See the citation note for claims 4 and 21 above.*

13. **As per claim 12**, Damron discloses a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the data processing system comprising:

first determining means, responsive to loading of an instruction in the code into a cache, for determining, by a processor unit, whether metadata for a prefetch is present for the instruction (col. 4, lines 58-61; col. 5, lines 17-24; Fig. 1, element 175; Fig. 3, element 220); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

second determining means, responsive to determination of metadata being present for the instruction, for determining whether data is to be prefetched (col. 5, lines 27-35; Fig. 3, element 230); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

and prefetching means, responsive to a determination that data is to be prefetched, for prefetching data, from within a data structure using the metadata, into the cache in the processor (col. 5, lines 24-26 and 35-42; Fig. 3, elements 225 and 235). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer.*

14. **As per claim 15**, Damron discloses retrieving means for retrieving the data from within the data structure using a pointer and an offset value (col. 5, lines 20-21). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 4 and 21 above.*

15. **As per claim 16**, Damron discloses retrieving means for retrieving the data from the data structure using an address (col. 5, lines 20-21). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer.*

16. **As per claim 17**, Damron discloses the processor unit is selected from one of an instruction cache or a load/store unit (col. 4, lines 58-61; Fig. 1, element 175). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means*

as a computer. Also, see the citation note for the similar limitation in claims 6 and 23 above.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 2, 13, and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Damron in view of Ishimi et al. (U.S. Patent 5,708,803).

19. **As per claims 2 and 19**, Damron discloses all the limitations of claims 2 and 19 except determining whether a number of outstanding cache misses is less than a threshold;

and wherein the prefetching step comprises:

prefetching the data when it is determined that the number of outstanding cache misses is than the threshold.

Ishimi discloses determining whether a number of outstanding cache misses is less than a threshold (col. 13, line 30; Fig. 13, element S4).

and wherein the prefetching step comprises:

prefetching the data when it is determined that the number of outstanding cache misses is than the threshold (col. 13, lines 30-32; Fig. 13, element S10). *It should be noted that the threshold is equal to 1. Thus, when it is determined there is a cache hit,*

meaning there are zero outstanding cache misses (i.e. the number of outstanding cache misses is than the threshold of 1), data is prefetched.

Damron and Ishimi are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Ishimi's fetch mechanism within Damron's data processing system.

The motivation for doing so would have been to provide a data processor capable of processing quickly by lessening the number of abortions even when a branch prediction is preformed (Ishimi, col. 3, lines 3-6).

Therefore, it would have been obvious to combine Damron and Ishimi for the benefit of obtaining the invention as specified in claims 2 and 19.

20. **As per claim 13**, the combination of Damron/Ishimi discloses first means for determining whether a number of outstanding cache misses is less than a threshold (Ishimi, col. 13, line 30; Fig. 13, element S4).

and wherein the prefetching means comprises:

second means for prefetching the data when it is determined that the number of outstanding cache misses is than the threshold (Ishimi, col. 13, lines 30-32; Fig. 13, element S10). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation notes for claims 2 and 19 above.*

21. Claims 3, 14, and 20 are rejected under 35 U.S.C. 103(a) as being obvious

over Damron in view of Hooker (U.S. Patent Application Publication 2003/0191900).

22. **As per claims 3 and 20**, Damron discloses all the limitations of claims 3 and 20 except determining whether a number of cache lines to be replaced is greater than a threshold;

and wherein the prefetching step comprises:

prefetching the data when it is determined that the number of cache lines chosen to be replaced is greater than the threshold.

Hooker discloses determining whether a number of cache lines to be replaced is greater than a threshold (paragraph 0069; Fig. 5, element 536); *It should be noted that the "response buffers" are analogous to the "cache lines."*

and wherein the prefetching step comprises:

prefetching the data when it is determined that the number of cache lines chosen to be replaced is greater than the threshold (paragraph 0070; Fig. 5, element 538).

Damron and Hooker are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hooker's microprocessor into Damron's data processing system.

The motivation for doing so would have been to reduce software code size over conventional single-cache line prefetch instructions because fewer prefetch instructions need to be included in the program (Hooker, paragraph 0018). Another motivation for

doing so would have been to potentially improve system performance by making more efficient use of the processor bus than the conventional method (Hooker, paragraph 0018). Lastly, another motivation for doing so would have been to potentially improve processing performance by moving data into the microprocessor cache more efficiently than the conventional method by alleviating the problems caused by the fact that a range of core clock to processor bus clock ratios may exist (Hooker, paragraph 0018).

Therefore, it would have been obvious to combine Damron and Hooker for the benefit of obtaining the invention as specified in claims 3 and 20.

23. **As per claim 14**, the combination of Damron/Hooker discloses first means for determining whether a number of cache lines to be replaced is greater than a threshold (Hooker, paragraph 0069; Fig. 5, element 536); *See the citation note for the similar limitation in claims 3 and 20 above.*

and wherein the prefetching means comprises:

second means for prefetching the data when it is determined that the number of cache lines chosen to be replaced is greater than the threshold (Hooker, paragraph 0070; Fig. 5, element 538).

Response to Arguments

24. Applicant's arguments filed January 5, 2007 with respect to **claims 1, 4-8, 12, 15-18, and 21-23** have been fully considered but they are not persuasive.

25. Applicant's arguments filed January 5, 2007 with respect to **claims 2-3, 13-14, and 19-20** have been considered but are moot in view of the new grounds of rejection above.

26. With respect to Applicant's argument beginning in the last paragraph on page 7 through the last paragraph of page 8 of the communication filed January 5, 2007, the Examiner respectfully disagrees. The Examiner refers Applicant to the rejection of claims 1, 12, and 18 above. As clearly shown in the citations of Damron, after the associated memory receives a prefetch request (i.e. responsive to loading an instruction in the code into a cache), the prefetch engine examines the termination value associated with the prefetch request to determine whether the termination value has a certain value (i.e. the prefetch unit determines whether metadata for a prefetch is present for the request). Next, the termination value is compared to either the address of last node that was prefetched or the number of nodes already prefetched in order to determine whether a termination condition has been satisfied (i.e. responsive to a determination of metadata being present for the instruction, determining whether data is to be prefetched). When a termination condition has been satisfied prefetching of data is terminated. However, when a termination condition has not been satisfied, data is to be prefetched and step 225 is repeated which involves prefetching data in a node (depending on the starting address and offset value of the prefetch request) and writing the data from the node into cache 160 (i.e. responsive to a determination that data is to be prefetched, prefetching data, from with a data structure using the metadata, into the cache in the processor). Accordingly, Damron sufficiently discloses responsive to

loading an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction, and responsive to a determination of metadata being present for the instruction, determining whether data is to be prefetched. Responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor.

27. As for Applicant's arguments with respect to independent claims 12 and 18, the arguments rely on the allegation that independent claim 1 is allowable and therefore for similar reasons independent claims 12 and 18 claims are allowable. However, as addressed above, independent claim 1 is not allowable, thus, Applicant's arguments with respect to independent claims 12 and 18 claims are not persuasive.

28. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that independent claims 1, 12, and 18 are allowable and therefore, by virtue of their dependency, the dependent claims are allowable. However, as addressed above, independent claims 1, 12, and 18 are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-8 and 12-23** have received a second action on the merits and are subject of a second action final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,544,342 (Dean) discloses a method and system are provided for prefetching information in a processing system.

2. U.S. Patent 5,603,004 (Kurpanek et al.) discloses a method for decreasing time penalty resulting from a cache miss in a multi-level cache system.

3. U.S. Patent 6,832,296 (Hooker) is the corresponding U.S. Patent to U.S. Patent Application Publication 2003/0191900 used in the rejections above.

4. U.S. Patent 6,848,030 (Tokar et al.) discloses a method and apparatus for filling lines in a cache.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
March 24, 2007

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